The importance of using dual channel heterostructure in strained P-MOSFETs

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***Abstract*— We present in this work a dual channel heterostructure strained structure, introduce the high carrier mobility Awaited in heterostructure devices while using several models which are : CVT, SHIRAHATA and WATT, we present a two dimensional simulation of dual strained channel heterostructure P-MOSFETs. This study is accomplished using SILVACO-TCAD simulation software, the comparison of the effect of using strain technique on P-MOSFET transistors will demonstrate the importance of using strain technique especially in dual channel heterostructure MOSFET. The simulation of fabrication steps and the extraction of the electronic proprieties in terms of transfer and output characteristics, transconductance, and the quasi-static capacitance allow understanding and interpreting these enhancements.**

***Keywords*—Strained Silicon; SiGe layer; MOSFET; Heterostructure; Simulation; SILVACO.**

I. INTRODUCTION

Strain is one among several solutions recognized by the organization of ITRS, as very promising and important material to continue the classical scaling based on the Moore law. [1]

Several researchers reported that strain technique enhance carriers mobility, the drive current, the transconductance and the saturation current. Strain Si heterostructure MOSFET transistor grown on relaxed SiGe substrate, demonstrate important carriers mobility improvements comparing to the bulk silicon [2-3-4].

The design of strained heterostructure MOSFET studied show enhancement in performances of both N and P-MOSFETs. However, researchers notice that the improvements in N-MOSFET structure are higher than those achieved in P-MOSFET structure, and this is due to hole mobility improvement that is far away lower than electron mobility improvement.

A combination between compressively strained $Si_{1-y}Ge_Y$ with tensile strained silicon grown on relaxed Si1-xGex, offers almost symmetric electron and hole mobility.

When we grow a thin silicon layer on $Si_{1-x}Gex$ layer, we create a biaxial strain silicon. In figure Fig. 1, we can notice that, when the lattice constant of silicon is inferior comparing to the lattice constant of germanium, the atoms of the silicon layer will be aligned with the atoms of Si1-xGex layer. The modification of the inter-atomic spacing induce several changes, among them; the band structure change, the states density, and the mobility of both kind of carriers.

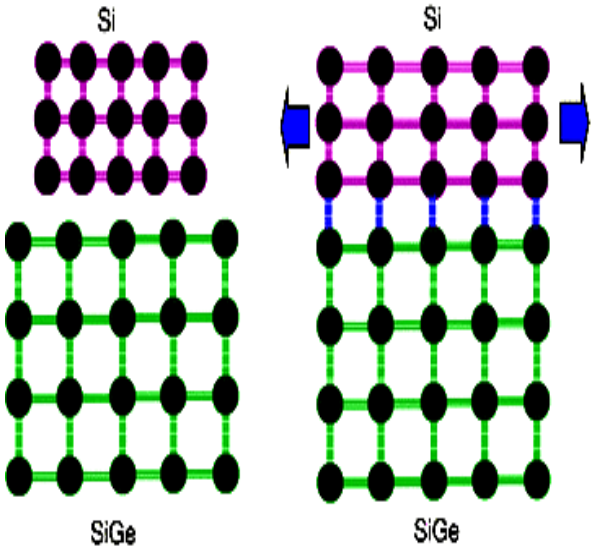

Fig. 1. Schematic of two layers, the Si layer is tensile strained.

By the same principle, compressive strain Si1−xGex is created by the growth of thin layer of $Si_{1-x}Ge_x$ on top substrate of silicon , as shown in figure Fig. 2.

Fig. 2 represents a dual strained channel heterostructure P-MOSFET.

It has been reported that we can obtain at same time both high electron and hole mobility enhancements in dual-channel structures. Strained silicon layer allow to have a high electron mobility and, strained SiGe channel allows to have a high-hole mobility channel.

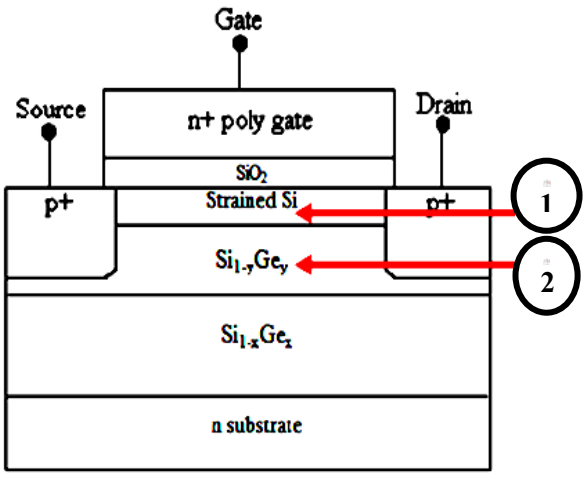

Fig. 2. Biaxially strained dual channel heterostructure P-MOSFET.

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II. Results and Discussions

We used ATHENA and ATLAS, two modules of SILVACO TCAD simulation software to simulate the fabrication steps and draw out the electronic characteristics of dual channel hetero-structure P-MOSFETs.

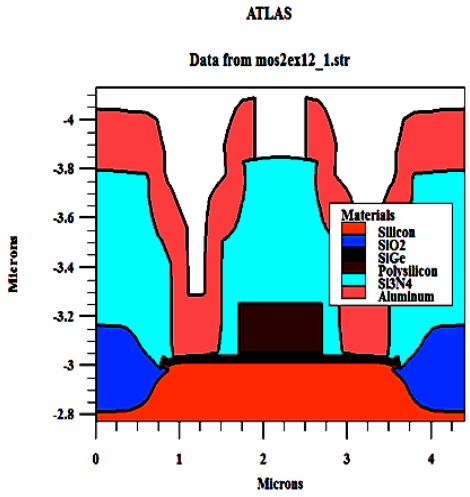

Fig. 3. SILVACO TCAD example of SiGe PMOS Process and Device Simulation

The simulated dual channel heterostructure is presented in figure Fig. 4.

Meshing in ATLAS is one of the most important step in process simulation. Poor meshing generally leads to simulation failure and can lead to inaccurate results that is why we refined the meshing in the channel region as it is shown in figure Fig. 5.

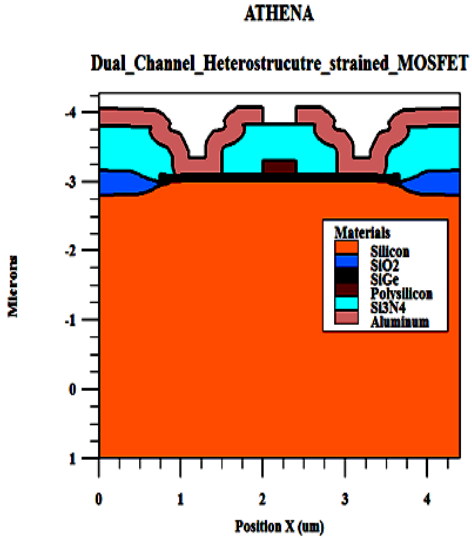

Fig. 4. The simulated dual channel strained heterostructure. Using ATHENA.

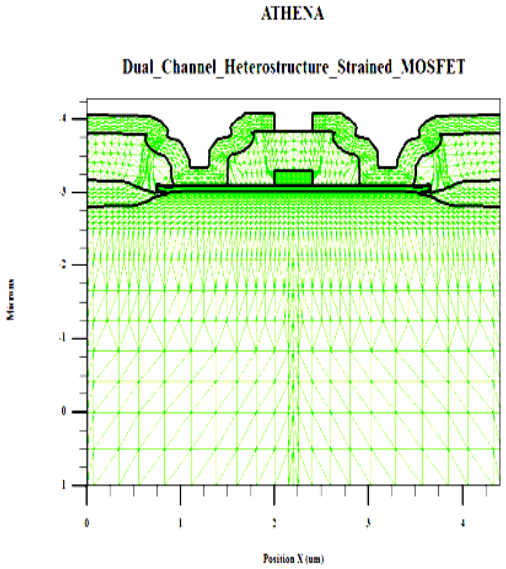

Fig. 5. The Mesh initialization of dual channel strained heterostructure. Using ATHENA.

Meshing in ATLAS is one of the most important step in process simulation. Poor meshing generally leads to simulation failure and can lead to inaccurate results that is why we refined the meshing in the channel region as it is shown in figure Fig. 5.

Fig. 6 shows doping profile obtained through our simulation. Reducing channel doping increases MOSFET mobility leading to increase SCEs. However, increasing doping level improves the control SCEs, but the channel mobility is reduced, our choice was a middle solution between the two possibilities.

We got the gate capacitance, Cg versus gate voltage in Fig. 7, by varying the V_{gs} between -3V and 3V with V_{Step} equal to 0.2V.

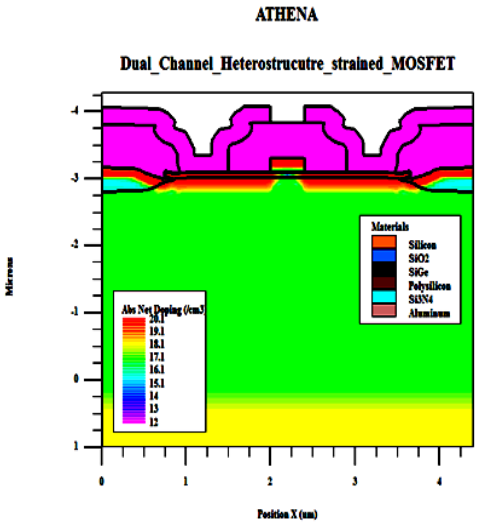

Fig. 6. Doping profile of dual channel strained heterostructure. Using ATHENA.

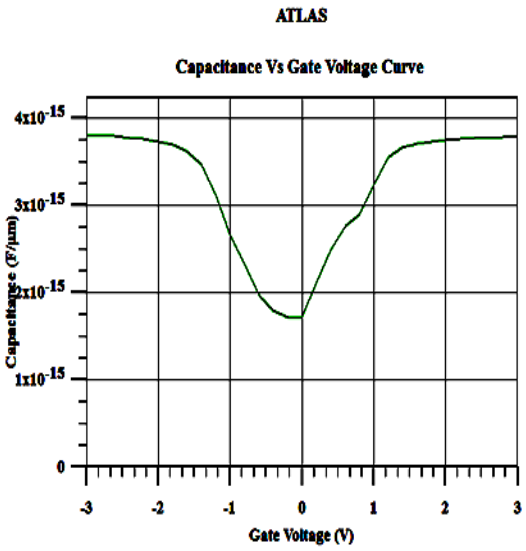

Fig. 7. The gate capacitance curve. Using ATLAS.

We noticed that dual channel strained structure shows a good Cg-Vgs characteristic, we do not notice interface density trapped between silicon cap and SiO2.

In Fig. 8, we represent the comparison between the transfer characteristics in classical MOSFET and dual channel heterostructure strained MOSFET.

For the Ids versus Vgs curve for dual channel heterostructure strained and conventional PMOS, the device was biased with the values respectively of -0.1V and -1.0V, which represents the minimum and maximum of the range values, the gate voltage vary from 1.0V to -2.0V with a V_{step} of -0.2V. From results we can notice that the strained silicon have an inferior threshold voltage than conventional one. This means that the transistor require low voltage to switch from off to on state. The strained MOSFET has a lower power use than conventional MOSFET.

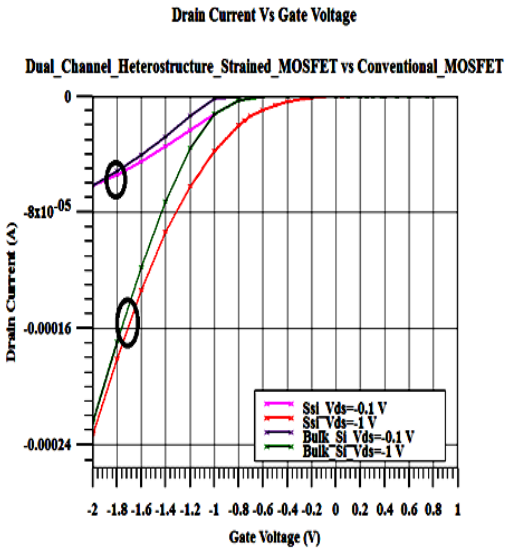

Fig. 8. Comparison of transfer characteristics in conventional and dual channel heterostructure strained MOSFET. Using ATLAS.

In Fig. 9, we represent the comparison of output characteristics in classical and dual channel heterostructure strained MOSFET.

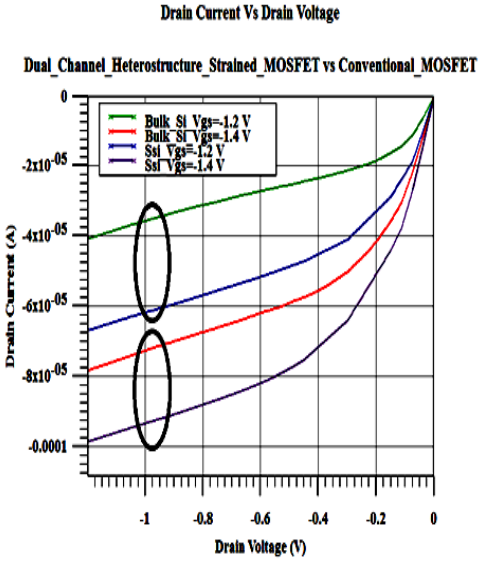

Fig. 9. Comparison of output characteristics in classical and dual channel heterostructure strained MOSFET. Using ATLAS.

From figure Fig.9 we notice an impressive enhancements obtained in dual channel heterostructure MOSFET, and this is due as we mentioned before to the enhancements obtained in mobility not only of holes as we can notice in single channel strained MOSFET but also in mobility of electrons. The improvement in I_{ds} current induces improvement in speed performance.

Our results confirmed the research studies in which it is reported that a high mobility is obtained using the dual heterostructure. [5-6].

This enhanced results can be explain by the improvement of effective mobility that is given by:

$$\mu_{eff} = q.\tau/m^* \qquad (1)$$

q: is constant (the carriers charge), $1/\tau$: is collision rate of carriers, and m*: is effective mass.

Those enhancements are explained mainly by the decreasing of the effective mass m*. For the dual heterostructure strained MOSFET, firstly, compressive strain in the Si1-yGey separates the valence band degeneracy and decrease effective mass, secondly , the band adjust between Si1-yGey and Si1-xGex creates quantum well for holes in the strained Si1-yGey which contributes in the enhancements of holes mobility. In the other hand the tensile strained layer of silicon contributes of the enhancements of electron mobility and that is exactly what we mentioned before.

The figure Fig.10 represents the transconductance obtained while using Vds equal to -0.2 V, this result confirmed the increased transconductance in deep submicron strained silicon MOSFETs.

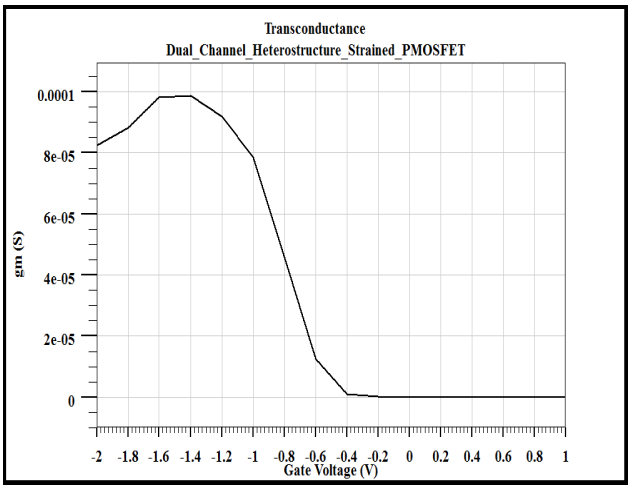

Fig. 10. The transconductance characteristic of Strained PMOSFET.

The figure Fig.11 represents the channel electron mobility extracted from the dual channel heterostructure strained PMOSFET and shows a good characteristic and high values of mobility.

To study the impact of the models on mobility, we used two other models, which are SHIRAHATA and WATT as it is shown in figures Fig.12 and Fig.13. WATT model take in consideration phonon scattering, surface roughness scattering, and charge impurity scattering induced by the inversion carriers [7].The SHIRAHATA model includes coulombic scattering [8]. Lombardi model [8] takes in consideration phonon and surface roughness, and effects of parallel and perpendicular electric field. In addition, We notice that WATT method allows attaining a higher level of mobility comparing to CVT and SHIRAHATA only in specified region and mobility equal to zero in the rest of structure, so we can say that CVT model is the most adequate to study the mobility in strained structure.

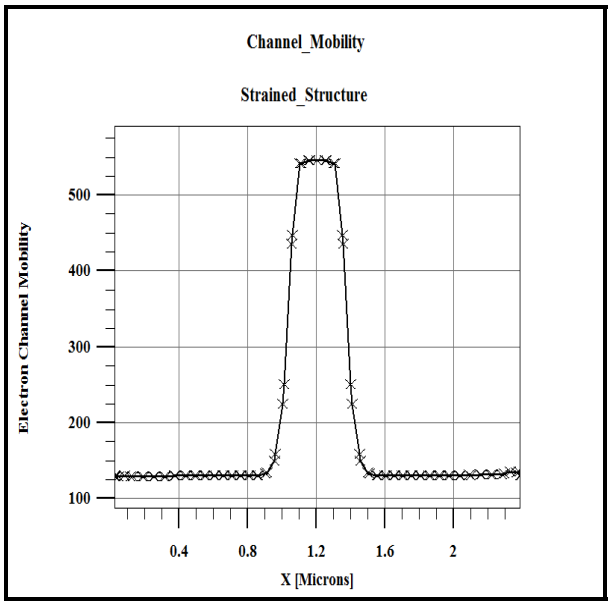

Fig. 11. Channel mobility extracted from strained structure .Using CVT model.

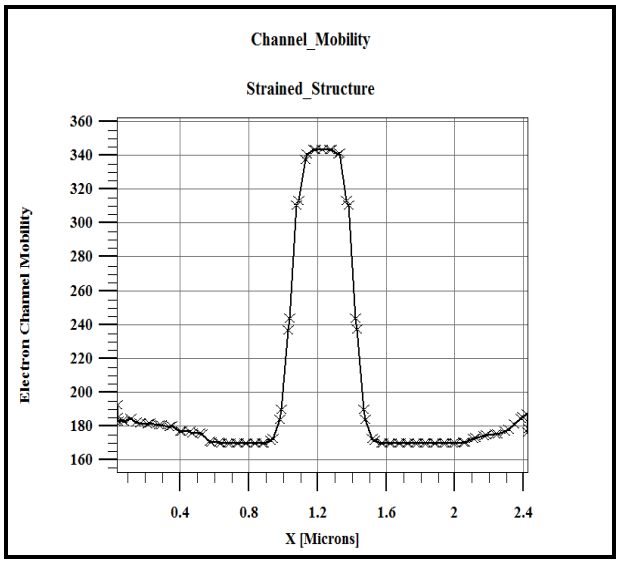

Fig. 12. Channel mobility extracted from strained structure .Using SHIRAHATA model.

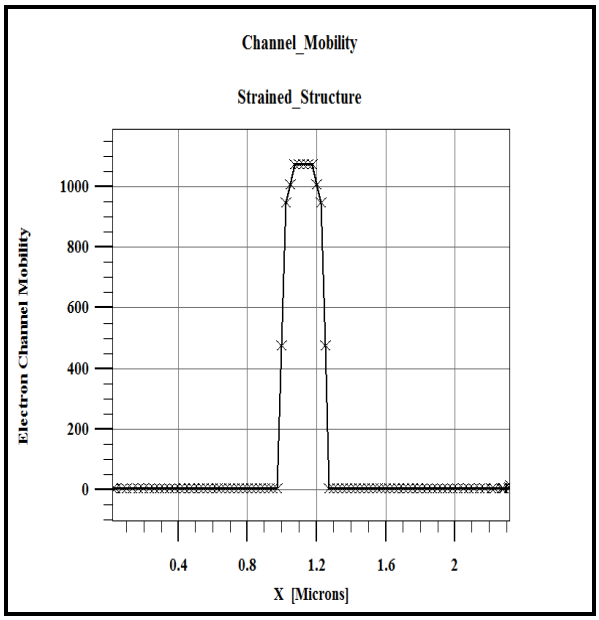

Fig. 13. Channel mobility extracted from strained structure .Using WATT model.

In figure Fig. 14, we represent the channel mobility versus the channel field in strained dual channel heterostructure PMOSFET.

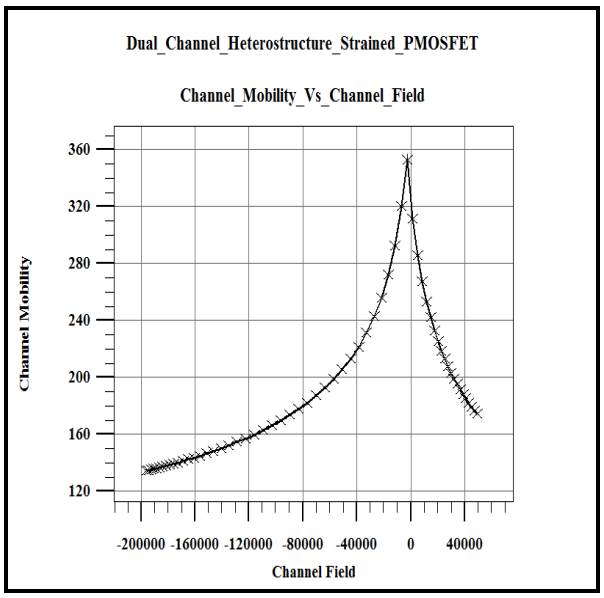

Fig. 14. Channel mobility versus channel field extracted from strained structure .Using ATLAS.

III. CONCLUSION

The results obtained after the extraction of the output characteristic, the transfer characteristic, and the capacitance gate curve, the transconductance in the dual channel heterostructure Strained P-MOSFETs, and the comparison with the conventional P-MOSFETs, we reported very important enhancements in terms of threshold voltage, drive current and saturation current. These enhancements allow optimizing the device performances, especially for logic applications, which need high speed switching with decreased threshold voltage and lower switching energy. These enhancements we can explain them by the enhancement of the channel mobility, the model of CVT is the model that allows to get the most important mobility and by result is the most adequate to study the impact of using strain silicon technology in MOSFET transistor. The aim of this work was to demonstrate that we can obtain the same level of enhancements in PMOSFET transistors as well as we can obtain in NMOSFET transistors, and this aim was attained trough the results obtained and presented.

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